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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/840,947	04/21/1997	EDWARD W. LIU	30454-21	2678

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/840,947	LIU, EDWARD W.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/30/04* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-8,10-14,16 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,10 and 27* is/are allowed.

6)☒ Claim(s) *1,3,4,6,11-14,16,20-26,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL REJECTION

Claim Rejections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6, 14, 16, 20, 21, 22, 24, 25, 26 and 29 are rejected under 35 USC 102(b) as being anticipated by Hadfield (US 5,038,215).

Hadfield discloses in Figures 5A-5B a noise canceller circuit comprising:

- a first circuit (51) having an input having a first input and a first output, wherein said first output includes a function of a signal at said first input and also includes a first noise component resulting from noise experienced by said first circuit;
- a second circuit (52) located proximal to said first circuit (51) and having a second input and a second output;
- a circuit (58) for supplying a signal to the second circuit (52) which results in a null output from the second circuit since the circuit (58) is a dummy readout register which generates only noise components;
- wherein said second output includes a function of a signal at said second input and also includes a second noise component resulting from noise experienced by said second circuit; and

- wherein the second noise component is approximately equal to the first noise component; a subtractor circuit (55) connected to said first circuit (51) and to said second circuit (52) to subtract said second output from said first output; and a digital circuit (53, 58) located proximate to said first circuit (51) and to said second circuit (52).

Note that, as shown on Figures 5A-5B of Hadfield, the amplifiers (51, 52) are identical so that the amplitude of noise are equal to perform the function. The amplifiers also experience noise by introducing and amplifying noise. The introduced noise comes from the components of the amplifiers and the amplified noise comes from the EMI noise coupled to the inputs of the amplifiers.

Claims 11-12 and 28 are rejected under 35 USC 102 (b) as being anticipated by Tanaka (JP406022007).

Tanaka discloses in Figures 1 and 7 a noise canceller circuit comprising:

- a plurality of analog circuits (5, 9), each proximal to each other, and each of said plurality of analog circuits producing an output signal which includes a function of an input signal and also includes a noise component resulting from noise experienced by said plurality of analog circuits;
- a noise separator circuit (12, 13), proximal to said plurality of analog circuits, and producing a noise signal based on noise experienced by said noise separator circuit;
- wherein the noise signal is approximately equal to the noise component of the output signal output by each of the plurality of analog circuits; and

- a noise canceling circuit (11) comprising a subtractor (18, Figure 7) which processes said output signals with said noise signal to reduce the noise component of the output signal output by each of the plurality of analog circuits (5,9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 6 are rejected under 35 USC 103 (a) as being unpatentable over Hadfield (5,038,215).

Hadfield discloses a noise canceller circuit in Figures 5A-5Bwith all of the limitations of the claimed invention as discussed above but does not disclose that the subtractor comprising a haft circuit which inputs a signal having an input amplitude and outputs an signal at one-half the input amplitude. For example, the present specification admits on lines 22-26 of page 6 that it is well known in the art to use the half circuit as the subtractor circuit. Thus, employing the half circuit in the circuit of Hadfield is considered to be a common practice for an engineer or a design expedient for an engineer depending upon a particular application. Lacking of showing any criticality, it would have been obvious to a person having skill in the art to employ the haft circuit in the circuit of Hadfield at the time of the invention for the purpose of accommodating with the requirement of a particular application.

With regard to claim 6, a skilled artisan recognizes that all components in Figures 5A-5B of Hadfield can be implemented on an integrated circuit for purpose of reducing size. Thus, it would have been obvious to a person having skill in the art at the time the invention was made to implement the circuit of Hadfield on an IC for reducing size .

Claim 23 is rejected under 35 USC 103 (a) as being unpatentable over Hadfield (US 5,038,215) in view of Tanaka (JP06022007).

Hadfield discloses in Figures 5A-5B a noise canceller circuit with all of the limitations of the claimed invention as discussed above but does not disclose that the subtractor is the digital circuit. Tanaka teaches in Figure 1 a noise canceller circuit comprising a digital subtractor (11) for subtracting digital inputs. It would have been obvious to a person having skill in the art at the time the invention was made to employ the digital subtractor taught by Tanaka in the circuit of Hadfield for the purpose of subtracting the digital input signals.

Claim 13 is rejected under 35 USC 103 (a) as being unpatentable over Tanaka (JP06022007).

Tanka discloses a noise canceller circuit in Figure 1 with all of the limitations of the claimed invention as discussed above but does not disclose that the subtractor comprising a haft circuit which inputs a signal having an input amplitude and outputs an signal at one-half the input amplitude. For example, the present specification admits on lines 22-26 of page 6 that it is well known in the art to use the half circuit as the subtractor circuit. Thus, employing the half circuit in the circuit of Tanaka is considered to be a common practice for an engineer or a design expedient for an engineer depending upon a particular application. Lacking of showing any

criticality, it would have been obvious to a person having skill in the art to employ the haft circuit in the circuit of Tanaka at the time of the invention for the purpose of accommodating with the requirement of a particular application.

Response to Applicant 's Arguments

The applicant argues that the readout registers (53, 58) of Hadfield are not the digital devices. The argument is not persuasive because, as well known in the art, the register of Hadfield in Figure 1 is the digital circuit since it is formed with flip-flops (G1-GN). Moreover, the input signal into the first flip-flop (G1) and the output signal at the output of the flip-flop (GN) are the digital signals because they are the squarewaves comprising two separate values of high (1) and low (0).

The applicant argues that the processor (11) of Tanaka does not process the microphone output signals. The argument is not persuasive because Figure 5 of Tanaka shows the first circuit (5) and the second circuit (9) coupled to the processor (11) through the A/D converters (12, 13) to cancel noise introduced to the first and second circuits (5, 9). There is nothing recited in claims 11-13 and 28 about the noise canceling circuit is a digital circuit.

The applicant argues that Haldfield does not disclose that a signal which is supplied to the second circuit (52) resulting in a null output from the second circuit. The argument is not persuasive. As shown in Figure 5a-5B of Hadfield, the output signal of the amplifier (52) is the null output because the dummy readout (58) generates just noise components so that the output of the second circuit (52) contains only noise (no real signal).

Allowable Subject Matter

Claims 7-8, 10 and 27 are allowable because the prior art does not show a signal supplying circuit supplying to the second input a signal which is an inverse of the signal at the first input.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 19, 2004

DINH T. LE
PRIMARY EXAMINER